UNITED STATES PATENT APPLICATION

of

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for

CONTACT INTEGRATION METHOD

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CONTACT INTEGRATION METHOD

[001]   This is a divisional of U.S. Application Serial No. 09/007,949, filed on January 16, 1998, which is a divisional of U.S. Application Serial No. 08/811,124, filed on March 3, 1997, now U.S. Patent No. 6,593,657 B1.

BACKGROUND OF THE INVENTION

1.   The Field of the Invention

[002]   The present invention relates to methods of making a plug and metallization line structure in microelectronic devices. More particularly the present invention relates to methods of minimizing resistance in the interface between plugs or contacts and the metallization lines connected to them. The present invention is also particularly drawn to methods of minimizing electromigration due to minimized interface resistance and selected alloying. The present invention is also drawn to improving depth-of-focus restrictions in the process of connecting plugs or contacts to metallization lines.

2.   The Relevant Technology

[003]   The process of forming contacts in semiconductors and the subsequent wiring of those contacts have several technical obstacles. These obstacles arise during fabrication and may be due to the use of differing materials. Some obstacles include depth-of-focus photolithographic problems, dissimilar metal-metal interface problems, electromigration problems, and irregular or large grain formation problems.

[004]   One technical obstacle is depth-of-focus photolithographic requirements in metallization line formation. Formation of metallization lines follows contact plug formation. During contact plug formation, a metallization line used to form the plug

may have a non-planar and irregular surface above the contact hole where the plug is to be formed. The non-planarity of the metallization layer is due to the use of a portion of the metallization material that is needed to fill up the contact hole. Non-planarity, and the rough topography of the metallization layer, causes depth of focus problems in subsequent photolithography steps. These problems cause irregular metallization line widths that lead to unpredictable resistances along the metallization lines, as well as unreliable device speeds.

[005]   The problem of a rough surface can be ameliorated by reflow methods, but even with reflow, there remains an uneven surface topography.

[006]   Another technical obstacle is resistance in metal-to-metal interfaces between plug and metallization line. This obstacle arises when two disparate metals make up the plug and metallization line, respectively, or even when two metals of the same composition are poorly interfaced. The process of forming contacts in semiconductors and the subsequent wiring of those contacts to form a completed integrated circuit conventionally comprises two steps. The first step comprises forming titanium or tungsten plugs that are filled into contact holes by such methods as cold or hot deposition, cold-slow, or hot-fast force filling, or metal reflow into the contact holes, followed by an etchback that leaves only titanium or tungsten plugs isolated in the underlying silicon substrate. The second step comprises forming a metallization line over the plugs.

[007]   Electrical conduction at the titanium or tungsten interface with the metallization line can be poor in that a completely connected interface area is difficult to substantially achieve, particularly where dissimilar metals are involved. Because resistance in electrical conduction is a function of cross-sectional area through a

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conductive body, a less than completely connected interface between plug and metallization line causes a higher resistance than that contemplated by the design geometries of the plug-to-metallization line surface area interface. In addition to incomplete interfacial contact, filling contact holes with titanium or tungsten requires high temperatures and pressures that cause large or irregular grain structures to grow. These large or irregular grain structures resist flow and etchback and do not conduct current as well as fine-grained structures.

[008]   Still other technical obstacles are electromigration and metal creep. These involve the transport of metal atoms opposite the direction of electron flow in the lines, and can lead to failure of the lines.

[009]   Al-Cu electromigration in a structure with Al-Cu metallization lines and Ti or W plugs is well established. The phenomenon occurs because Cu diffusivity through Ti or W is much lower than through Al. Therefore the Cu is depleted from the area of the Ti or W plug by the current flow and not replaced, leading to failure at the interface between the Ti or W plug and the Al-Cu metallization lines.

[010]   Metal creep, on the other hand, occurs due to the differences in the thermal coefficients of expansion between metals, insulators, and silicon wafers. The differences in thermal coefficients of expansion can build up stress in the metallization lines, which can lead to migration of atoms in the metallization line to the various areas of high stress and strain. This migration of atoms forms voids or vacancies in the metallization line which can cause creep failure. Additional solutions which can control both the electromigration and metal creep problems are desirable.

[011]   Yet another technical obstacle involves large or irregular grain growth during the formation of metallization lines. Large or irregular grain growth can be

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caused by high processing temperatures, a high contact channel density in a dielectric substrate, and the interfaces between disparate metals. For example, where a wetting surface layer is placed upon a substrate to assist in metal flow, interaction between the wetting surface layer and the metallization material can result in large or irregular grain growth.

[012] In the case of a titanium or titanium nitride wetting surface layer, an aluminum metallization layer can react with the wetting surface layer to cause titanium aluminide intermetallic combinations that have large grain cluster formations. Large grain structures adversely affect reflow capabilities and resist planarization. Such adverse effects prevent proper plug filling and the result is poor electrical conductivity and slower and less reliable devices.

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SUMMARY OF THE INVENTION

[013]   The present invention is drawn to methods of making a semiconductor substrate having thereon plug or contact connections to metallization lines, which methods minimize electrical resistance, relieve depth-of-focus restrictions during patterning of the metallization lines, and resist electromigration and creep failure between the plug or contact and the metallization line. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive material, including but not limited to bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term "substrate" refers to any supporting structure including but not limited to the semiconductor substrates described above.

[014]   A first method of the present invention comprises patterning a contact hole within an insulation layer situated on a semiconductor substrate or equivalent. The contact hole can be for a via, interconnect, or bit line. A first metal layer is then formed upon the insulation layer. If necessary for complete filling of the contact hole, additional steps are carried out by such methods as reflow or pressure fill. The first metal layer is then planarized to isolate a plug of the first metal layer in the contact hole within the insulation layer. After isolating the plug in the contact hole, a second metal layer is formed upon the insulation layer over and on an exposed end of the isolated plug. The second metal layer may then be planarized to a preferred thickness so as to render the same with a photo-notching resistant surface that alleviates stringent depth-of-focus requirements in forming metallization lines. Finally, metallization lines are

patterned out of the second metal layer. The first and second metal layers can be composed of either a substantially pure metal or an alloy thereof.

[015]   A second method of the present invention comprises patterning a contact hole within an insulation layer situated on a substrate assembly or equivalent. A single layer of metal is then formed upon the insulation layer. If necessary for complete filing of the contact hole, additional steps are carried out by such methods as reflow or pressure fill. The single layer of metal is then planarized above the insulation layer to a thickness that is preferred for metallization lines. Finally, the single layer of metal is patterned to create therefrom a unitary structure of both metallization lines and a plug isolated in the contact hole of within the insulation layer. The single layer of metal can be composed of either a substantially pure metal or an alloy thereof.

[016]   A third method of the present invention comprises the same processing steps for the first metal layer. Selection of alloys of the first and second metal layers is required in the third method in which a heat treatment, after formation of the second metal layer, causes preferred metal species diffusion between the two metal layers. The preferred diffusion causes a substantially uniform concentration gradient at the interface between the first and the second metal layers that minimizes resistance, creep failure, and electromigration. The heat treatment can either precede or follow planarization of each of the first and second metal layers.

[017]   As an optional series of steps for any of the foregoing three methods, the contact hole can be filled with a plug of conductive material other than aluminum. The conductive material of which the plug is formed preferably comprises, but is not limited to, tungsten. It is also preferred that, prior to depositing the tungsten or other conductive material, a liner layer of a refractory metal nitride is first deposited. The

refractory metal is deposited in an atmosphere of nitride and is subsequently annealed to

serve as a barrier to prevent diffusion and chemical attack of the chemistry used to

deposit the tungsten or other conductive material. The metal nitride is typically

annealed to form a metal silicide at an interface with an underlying silicon substrate and

to improve barrier properties of the metal nitride. The plug material is then deposited as

described for one of the foregoing methods.

[018]   These and other features of the present invention will become more fully

apparent from the following description and appended claims, or may be learned by the

practice of the invention as set forth hereinafter.

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BRIEF DESCRIPTION OF THE DRAWINGS

[019]   In order to illustrate the manner in which the above-recited and other features of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

[020]   Figure 1 is a cross-sectional view of a planarized insulation layer having therein a contact hole, the insulation layer being situated on a semiconductor substrate, and a metallization layer being disposed upon the insulation layer over the contact hole which is not filled by the metallization layer.

[021]   Figure 2 is a cross-sectional view of the structure seen in Figure 1, where the metallization layer fills the contact hole, and the metallization layer has a non-planar top surface above the insulation layer.

[022]   Figure 3 is a cross-sectional view of the structure seen in Figure 2, where the metallization layer is planarized at the top surface of the insulation layer so as to isolate within the insulation layer a plug in the contact hole.

[023]   Figure 4 is a cross-sectional view of the structure seen in Figure 3, where a second metallization layer is formed over the insulation layer on and above the isolated plug in the contact hole, and also showing in a graphic form an optional thermal diffusion of a preferred alloying element from the second metallization layer into the first metallization layer in the contact hole.

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[024]   Figure 5 is a cross-sectional view of the structure seen in Figure 3, and further illustrates a partial etch of the insulation layer below the extent of the plug and thereby exposing lateral surfaces below the top surface thereof, followed by the formation of a second metal layer over the insulation layer and over the top and exposed lateral surfaces of the plug, the top surface of the second metal layer having been planarized to a preferred thickness suitable for metallization lines.

[025]   Figure 6 is a cross-sectional view of a planarized insulation layer having therein a contact hole, the insulation layer being situated on a semiconductor substrate, and a metallization layer being disposed upon the insulation layer over the contact hole filled by the metallization layer, the metallization layer having been planarized above the insulation layer to a preferred thickness suitable for metallization lines.

[026]   Figure 7 is a cross-sectional view of the structure seen in Figure 3, and further illustrates a refractory metal silicide layer at the bottom of the contact hole, the contact hole being lined by a refractory metal nitride layer, the plug being in contact with both the refractory metal silicide layer and the refractory metal nitride layer, and a second metal layer over the insulation layer and over the top of the plug, the refractory metal silicide layer, and the refractory metal nitride layer, the top surface of the second metal layer having been planarized to a preferred thickness suitable for metallization lines.

[027]   Figure 8 is a section taken along the line 8--8 from Figure 7 in which the contact plug has a second end opposite the first end in contact with the refractory metal silicide layer at the bottom of the contact hole; the second end is in contact with a second refractory metal silicide layer, the second refractory metal silicide layer being in contact with the metallization line.

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DETAILED DESCRIPTION OF THE INVENTION

[028]   The present invention comprises methods to overcome technical challenges in the prior art and structures achieved thereby. Materials used in the present invention are preferred but are illustrative of non-limiting examples by which the present invention can be carried out with equivalent materials, either by resort to the specification or by practicing the invention as disclosed herein.

[029]   A preferred material in the methods of the present invention is boron phosphorus silicate glass (BPSG) for an insulation layer in which a contact hole is provided. The insulation layer may also be composed of TEOS, doped silicon dioxide, BPSG, PSG, BSG, and silicon nitride, where TEOS is an oxide of silicon deposited in a chemical vapor deposition (CVD) process using a tetraethylorthosilicate precursor. The insulation layer is preferably situated on a semiconductor substrate of a semiconductor wafer. Other materials are dielectrics known in the art that are structurally sound so as to withstand processing conditions and field operating conditions. The dielectrics include, but are not limited to oxides, nitrides, carbides, carbon nitrides, oxynitrides, doped or slightly doped monocrystalline or polycrystalline silicon, and equivalents.

[030]   Metallization materials for both contact hole filling and metallization line formation can be chosen from known conductive materials. Preferred materials include aluminum and aluminum alloys of AlCu, AlSi, AlSiCu, AlTi and equivalents. Other aluminum alloys that are contemplated as consistent with the present invention include AlAg, AlAu, AlMn, AlNa, AlW, AlCuZn, AlNi and equivalents.

[031]   Because aluminum has a melting point of about 660 °C, substantially lower than that of tungsten (3,370 °C) or titanium (1,800 °C), achieving ductility sufficient to cause pressure or reflow filling of the contact hole comes at significantly lower

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temperatures for aluminum. For example, aluminum alone has a melting point that is about 26 percent of the melting point of tungsten, about 37 percent of the melting point of copper, and about 46 percent of the melting point of silicon. Adding preferred amounts of copper and/or silicon alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill in the contact hole (about 57 percent of tungsten) or of tungsten plug fill in the contact hole.

[032]   Figure 1 illustrates the first step in the inventive method in which a semiconductor device 10 has an insulation layer 14 disposed upon a semi-conductive device underlying layer 12. A contact hole 16 has been formed, such as by patterning and etching, within insulation layer 14. Contact hole 16 exposes semiconductor substrate 12 and a first metallization layer 18 has been formed, such as by deposition, upon insulation layer 14.

[033]   Formation of first metallization layer 18 can be accomplished by physical vapor deposition (PVD), CVD, electroplating, and electroless plating. If first metallization layer 18 does not fill contact hole 16 when metallization layer 18 is formed, procedures for filing contact hole 16 are implemented. Various procedures are known to the art, such as pressure filling, reflow, and wetting layer-assisted reflow for CVD and PVD. For electroplating and electroless plating, the surface tension of the plating solution tended to resist the filling of a contact hole, particularly as the aspect ratio of the contact hole increases. As such, surfactants and/or other means of overcoming both surface tension and electrostatic charges must be employed to ensure that the contact hole is substantially completely filled.

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[034]   Figure 2 illustrates the result of a pressure filling step in filling contact hole 16 with first metallization layer 18. A topographical depression forms in first metallization layer 18 above contact hole 16, caused by the filling of first metallization layer 18 into contact hole 16. Removal of at least some of first metallization layer 18 is next required to planarize the same. After formation of first metallization layer 18, an optional heat treatment is carried out to anneal structure of semiconductor device 10.

[035]   Figure 3 illustrates the result of a planarization step that stops on insulation layer 14. The planarizing step can be either a mechanical planarizing step of a chemical mechanical planarization step (CMP). After the planarization step, only a contact plug 19 remains of first metallization layer 18. Contact plug 19, which is isolated by insulating layer 14, fills contact hole 16. A mechanical planarization step is costly in both time and materials. Mechanical planarization also requires a cleaning step before the wafer can be advanced to the next process step. If a chemical mechanical planarization process (CMP) is used to planarize and then stop on insulation layer 14, as shown in Figure 3, chemicals in the CMP process oxidize upper surfaces of first metallization layer 18 and abrasives therein shear away oxides of the upper surfaces of first metallization layer 18 in a repeating cycle that eventually planarizes first metallization layer 18.

[036]   Following planarization, a second metallization layer 20 seen in Figure 4 is formed upon insulation layer 14. Second metallization layer 20, like first metallization layer 18, can be formed by PVD, CVD, or variations thereof. Second metallization layer 20 is formed upon an exposed end of isolated contact plug 19. A second planarization step is carried out to planarize the exposed upper surface of second metallization layer 20. This second planarization step is performed until second

metallization layer 20 has of a preferred metallization line thickness. Like the first planarization step, the second planarzation step can be either a mechanical planarization step or a chemical mechanical planarization step.

[037]   By performing a second planarization step upon second metallization layer 20, the quality of planarity is achieved in which photolithographic restrictions upon depth-of-focus are ameliorated. Because of a planarity achieved by planarization that cannot be achieved merely by deposition, photographic notching is minimized as well as an irregular topography, both of which require a greater depth-of-focus.

[038]   After deposition of second metallization layer 20, an optional heat treatment step can be carried out to anneal both isolated contact plug 19 and second metallization layer 20.

[039]   Another method of the present invention, illustrated in Figure 6, involves forming sole metallization layer 22 upon insulation layer 14. If sole metallization layer 22 does not fill contact hole 16 when it is formed, procedures for filing contact hole 16 are implemented as described above. Planarization of sole metallization layer 22, such as by a mechanical or chemical-mechanical planarization process, is then undertaken. Planarization of sole metallization layer 22, however, does not expose insulation layer 14, but rather achieves a desired thickness upon insulation layer 14. Planarized sole metallization layer 22 and contact plug 19 are an integral structure, thus providing for one less metal-to-metal interface when compared with the structure see in Figures 4 and 5. Few metal-to-metal interfaces will correspondingly reduce resistance to current flow, in that a metal-to-metal interface may have discontinuities that cause resistance at the interface to be higher, which in turn causes the inherent inefficiency of Joule heating to occur.

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[040]   Another method of the present invention involves diffusive heat treating of isolated contact plug and second metallization layer 20. The procedures as set forth above for Figures 1-5 are followed. For first metallization layer 18, specific alloys are selected that allow for substantially complete filling of contact hole 16. In the case of second metallization layer 20, specific alloys are selected that allow for an excess of a preferred alloying element to be present. After the selection and use of the selected specific alloys in first and second metallization layers 18, 20, a heat treatment step is carried out following the formation of second metallization layer 20. The heat treatment is conducted for a time period sufficient to allow a selected amount of a preferred alloying element to diffuse from a region of higher concentration within second metallization layer 20 to a region of lower concentration in isolated contact plug 19.

[041]   The forgoing diffusion method can have the alternative of causing the diffusion from isolated contact plug 19 into second metallization layer 20.   For example, where first metallization layer 18 has sufficient ductility qualities to substantially fill contact hole 16, but responds poorly to planarization, diffusion of a preferred alloying element from isolated contact plug 19 into second metallization layer 20 will create a substantially uniform concentration gradient profile of a preferred alloying element, but will not have affected the second planarization process of second metallization layer 20.

[042]   Figure 4 illustrates, in the graph seen therein, one result of the diffusion methods set forth above. The result of the heat treatment and its induced diffusion is that a substantially uniform concentration gradient of the preferred alloying element is exhibited at an interface B between isolated contact plug 19 and second metallization layer 20. The graph in Figure 4 illustrates this substantially uniform concentration

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gradient of a preferred alloying element taken along the line A--A and including interface B. The graph depicts distance (X) from semiconductor substrate 12 toward second metallization layer 20 with respect to concentration (Y) of a preferred alloying element. In this embodiment, diffusion is illustrated as having proceeded from second metallization layer 20 into isolated contact plug 19. Diffusion, however, can also proceed from isolated contact plug 19 into second metallization layer 20.

[043]   A substantially uniform concentration gradient of a preferred alloying element can have various qualities. One quality is the reduction of electromigration when pure aluminum is used for both first metallization layer 18 and contact plug 19. The problem of electromigration of aluminum can be reduced in its effect when the alloying element is selected from the group of elements that resists aluminum electromigration, such as copper, silicon, titanium and other equivalents known in the art and achievable by routine experimentation.

[044]   Another quality is resistance to metal creep that is normally caused by physically interfaced metals of disparate thermal expansion coefficients. By causing a substantially uniform concentration gradient of a preferred alloying element between isolated contact plug 19 and second metallization layer 20, the tendency for metal creep is lessened as the composition at interface B, seen in Figure 4, can be substantially the same on both sides of interface B. Alternatively the composition on either side of interface B can be of two different types but with substantially equivalent coefficients of thermal expansion at B.

[045]   Another quality achieved in methods of the present invention is the avoidance of creating large and irregular grain structures in the metallization. These problematic grain structures are avoided when lower processing temperatures, such as

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those required for aluminum or a lightly-doped aluminum alloy, are used to fill contact hole 16. Because aluminum has a melting point of about 660 °C, substantially lower that of tungsten (3,370 °C) or titanium (1,800 °C), achieving ductility sufficient to cause pressure or reflow contact hole filling comes at significantly lower temperatures. For example, aluminum alone has a melting point that is about 26 percent that of tungsten, copper, about 37 percent, and silicon, about 46 percent. Adding preferred amounts of copper and/or silicon alloying elements does not significantly cause the pressure fill or reflow temperatures to materially approach those required of a titanium plug fill (about 57 percent of tungsten) or of a tungsten plug fill.

[046]   By maintaining lower temperatures, metal lines do not have the opportunity to form large or irregular grain structures. Such structures inhibit both metal reflow and planarization and are therefore to be avoided.

[047]   Another method of the present invention is illustrated in Figure 6. This method involves etching first metallization layer 18 to expose insulation layer 14, and then exposing lateral surfaces 24 of isolated contact plug 19. This method can be carried out by a single planarizing step, such as mechanical or chemical mechanical planarization, that will remove insulation layer 14 faster than first metallization layer 18 is removed, with some of each being removed by the planarizing step. When a chemical mechanical planarization step is used, the chemistry thereof requires that physically shearable surfaces are created in both first metallization layer 18 and in insulation layer 14, but that between these two the etch is more selective to first metallization layer 18 than insulation layer 14. An alternative to achieve the same structure with exposed lateral surfaces 24 is to stop on insulation layer 14 in a CMP step and conduct a second etch that is selective to isolated contact plug 19.

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[048] The methods illustrated in Figures 1-7 can be modified by forming a refractory metal nitride lining 26 and a refractory metal silicide layer 24 at an interface between contact plug 19 and semiconductor substrate 12. This modification allows the use of materials other than aluminum for forming contact plug 19. In one embodiment, a tungsten plug is formed. In so doing, a refractory metal nitride is deposited in contact hole 16 lining the sides of contact hole 16. The refractory metal nitride is then annealed. In the case where semiconductor substrate 12 comprises a silicon substrate, a refractory metal silicide layer 30 is formed at the bottom of contact hole 16 upon semiconductor substrate 12. The anneal also improves the barrier properties of the refractory metal nitride, which prevents diffusion and chemical attack of the chemistry used to deposit the tungsten or other conductive material. Tungsten is then deposited to form contact plug 19. The steps of depositing first metallization layer 18 follow with variations as proposed above with respect to Figures 1-8.

[049] The present invention also includes a contact plug and metallization line structure according to Figures 7 and 8. The contact plug and metallization line structure includes semiconductor substrate 12 having a contact surface thereon. It also includes insulation layer 14 having contact hole 16 therethrough extending to the contact surface of semiconductor substrate 12. Additionally, it includes contact plug 19 substantially composed of a first metal and situated in contact hole 16, contact plug 19 being electrically insulated by insulation layer 14. Second metallization line 20 is substantially composed of a second metal, wherein contact plug 19 and second metallization line 20 are electrically connected and have a substantially continuous composition gradient of a selected alloying element between the first metal and said second metal. The contact surface of semiconductor substrate 12 has first refractory

metal silicide layer 30 thereon in contact with a first end of the plug 19. Contact hole 16 has an inside wall upon which a refractory metal nitride layer is situated in contact with the insulation layer and the plug. Additionally, contact plug 19 has a second end opposite the first end and in contact with a second refractory metal silicide layer 34 as seen in Figure 8. Second refractory metal silicide layer 34 is in contact with second metallization line 20.

[050]   The present invention also includes a contact plug and metallization line structure. The contact plug and metallization line structure includes semiconductor substrate 12 having situated thereon a silicon layer with a contact surface thereon. It also includes insulation layer 14 of BPSG on the silicon layer. Additionally, it includes contact hole 16 extending through insulation layer 14 of BPSG to the contact surface on the silicon layer. In addition thereto, it includes a refractory metal silicide layer 30 of titanium silicide on the contact surface of the silicon layer. Additionally, it includes refractory metal nitride lining 26 of titanium nitride on a sidewall of contact hole 16. Contact plug 19 is substantially composed of a first metal selected from the group consisting of Al, AlCu, and AlSiCu, and being situated in contact hole 16. Contact plug 19 is in contact, at an end thereof, with refractory metal silicide layer 30 of titanium silicide. Contact plug 19 has a sidewall in contact with refractory metal nitride lining 26 of titanium nitride, and contact plug 19 is electrically insulated by insulation layer 14 of BPSG. Second metallization line 20 is substantially composed of a second metal selected from the group consisting of Al, AlCu, and AlSiCu. One of the first and second metals has a higher concentration of Cu than the other of the first and second metals. Contact plug 19 and second metallization line 20 are electrically connected and have a substantially continuous composition gradient of a selected alloying element

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between the first metal and the second metal, second metallization line 20 having a substantially planar top surface. Contact plug 19 has first and second opposite ends each of which is in contact with refractory metal silicide materials 30, 34, respectively.

[051]   The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

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